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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,495	02/11/2002	William A. Stevens, JR.	042390.P9143	6012
7590	07/14/2006		EXAMINER	
Lawrence E. Lycke BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP Seventh Floor 12400 Wilshire Boulevard Los Angeles, CA 90025-1026			CHEN, TSE W	
			ART UNIT	PAPER NUMBER
			2116	
			DATE MAILED: 07/14/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/073,495	STEVENS, ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 08 June 2006.
2a) This action is **FINAL**. 2b) This action is non-final.
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-41 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-41 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.

 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____.
4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 8, 2006 has been entered.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-2, 15-16, and 25-26 provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 3, 14, and 23 of copending Application No. 10112920. Claim 1 of Instant Application maps to claims 1 and 3 of said copending Application. Claim 2 of Instant Application maps to claim 1 of said copending Application. Claims 15-16 of Instant Application maps to claim 14 of said copending Application. Claims 25-26 of Instant Application maps to claim 23 of said copending Application. Although the conflicting claims are not identical with the Instant Application

utilizing a BIOS component, they are not patentably distinct from each other because the claims are directed to substantially the same subject matter involving firmware modules in a pre-memory execution environment.

Instant Application	US Application 10/112920
<p>1. A method comprising: starting execution of a basic input output system (BIOS), the BIOS including a plurality of modules; determining firmware resources required by each of the plurality of modules to operate, the firmware resources required, if any, for a given firmware module provided by one or more other firmware modules; scheduling modules of the plurality of firmware modules for execution in consideration of the required firmware resources that are determined; and dispatching the scheduled modules for execution.</p> <p>2. The method of claim 1, wherein the plurality of firmware modules are dispatched and executed in a pre-memory execution environment prior to a availability of system memory for a platform on which the BIOS is installed.</p> <p>15. A machine readable medium containing instructions that when executed by a machine, cause the machine to perform operations comprising: starting execution of a BIOS, the BIOS including a plurality of firmware modules; determining firmware resources required by each of the plurality of modules to operate, the firmware resources required, if any, for a given firmware module provided by one or more other firmware modules; scheduling modules of the plurality of firmware modules for execution in consideration of the required firmware resources that are determined; and dispatching the scheduled modules for execution.</p> <p>16. The machine readable medium of claim 15, wherein the machine comprises a platform including a processor on which the instructions are executed and system memory, further comprising instructions that when executed by the machine cause the machine to perform an operation of initializing the system memory of the platform after the scheduled modules are dispatched.</p> <p>25. A system, comprising: a plurality of hardware components; a first memory device to store a BIOS, the BIOS including a plurality of firmware modules, the BIOS further including; means for determining firmware resources required by each of the plurality of firmware modules to operate, the firmware resources required, if any, for a given firmware module provided by one or more other firmware modules, means for scheduling execution of modules of the plurality of modules, and means for dispatching scheduled modules for execution; and a processor on which the firmware modules are executed, coupled to the plurality of hardware components and the first memory device.</p> <p>26. The system of claim 25, wherein the BIOS further comprises means for initializing system memory of the system after the scheduled modules are dispatched.</p>	<p>1. A method comprising: identifying any services that must be produced prior to executing each of a plurality of firmware modules; identifying services produced by each of said plurality of firmware modules upon execution of that firmware module; and determining an execution order in which said plurality of firmware modules may be properly executed, said execution order being determined during an initialization process of a computer system prior to main memory for the computer system being accessible.</p> <p>3. The method of claim 1, wherein the operations of the method are implemented through a set of firmware instructions corresponding to a dispatcher that is executed during the initialization process.</p> <p>14. A machine-readable media on which a plurality of instructions are stored that when executed by a processor enable a computer system to perform the operations of: searching for firmware modules that contain firmware that is used to initialize the computer system during an initialization process; for each firmware module that is found, identifying any services that must be produced prior to executing that firmware module; identifying services produced by each of firmware modules upon execution of that firmware module; and dispatching the firmware modules for execution in an execution order that is determined during the initialization process prior to initializing main memory for the computer system, said execution order ensuring that any services required by each firmware module has been previously produced prior to dispatching that firmware module.</p> <p>23. A non-volatile memory component comprising: a boot firmware device on which a plurality of firmware instructions are stored, including, a set of instructions to perform early initialization of a computer system in which the boot firmware may be implemented upon execution of those instructions by a processor in the computer system, said early initialization being performed during a cold boot operation or in response to reset event; a set of instructions corresponding to a dispatcher that when executed by the processor performs the operations of, determining an execution order in which a plurality of firmware modules stored on the boot firmware device and/or one or more other firmware devices that may be accessed by the computer system may be properly executed based on service dependency requirements of each firmware module and services provided by each firmware module, said execution order being determined during an initialization process of the computer system that includes the early initialization and is prior to main memory for the computer system being accessible; and dispatching the firmware modules for execution by the processor based on the execution order.</p>

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Objections

3. Claims 1 and 15 are objected to because of the following informalities: “determining a subset of the plurality firmware modules that call the firmware module” should be “determining a subset of the plurality of firmware modules that call the firmware module”. Appropriate correction is required.

Claim Rejections - 35 U.S.C§ 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1-3, 13-17, 23-27, and 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens, U.S. Patent 6633976, in view of Stevens, "EFI A BIOS Vendor's Perspective", hereinafter ReStevens, and Sasaki et al., US Patent 6708271, hereinafter Sasaki.

6. In re claim 1, Stevens discloses a method comprising:

- Starting execution of a basic input output system (BIOS) [col.2, 11.14-29], the BIOS having a plurality of firmware modules [e.g., module to initialize CPU, module to initialize memory; typically stored in solid state non-volatile memory] [fig.2; col.2, 1.48 - col3, 1.15].
- Scheduling the plurality of firmware modules for execution [col.2, 1.48 - col.3, 1.15; col.3, 11.1-15; sequentially schedules modules for execution].

- Scheduling the plurality of firmware modules for execution [col.2, 1.48 - col.3, 1.15; col.3, 11.1-15; sequentially schedules modules for execution].
- Dispatching the scheduled plurality of firmware modules for execution [col.2, 1.48 - col.3, 1.15; col.3, 11.1-31].

8. Stevens did not disclose explicitly the determining of resources required by the plurality of modules nor the determination of callable firmware modules.

9. ReStevens discloses a method [extensible firmware interface] comprising:

- Determining firmware resources [EFI drivers] required by each of a plurality of firmware modules [EFI Option ROMs], the firmware resources required are associated with one or more other firmware modules [EFI PHASE 1, "Boot Process" slide; EFI drivers are firmware modules to be utilized as firmware resources by EFI Option ROMs].
- Scheduling the plurality of firmware modules for execution in consideration of the determined required firmware resources [EFI PHASE 1, "Boot Process" and "EFI Phase 1" slides; scheduling of firmware modules with incomplete loaded firmware resources would render the system inoperable]. Examiner takes official notice that it is well known in the art to schedule complete modules for proper execution [i.e., executing modules with missing drivers would render the system inoperable].

10. Sasaki discloses a method comprising determining a subset of the plurality of modules [firmware of Stevens] a module [communication manager] may call [in order to provide updates] and determining a subset of the plurality of firmware modules that call the module [in order to service request] [col.2, 1.50 – col.3, 1.5].

11. It would have been obvious to one of ordinary skill in the art, having the teachings of Sasaki, Stevens and ReStevens before him at the time the invention was made, to modify the

system of Stevens to include the well-known extensible firmware interface of ReStevens, in order to enhance the compatibility between legacy OS and current BIOS [ReStevens: "EFI Phase 1" slide]; and to include the teachings of Sasaki, as the determination of callable modules is well known in the art and suitable for use with the system of Stevens . One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to enhance the compatibility between legacy OS and current BIOS; and simplify the design of multi-module system [Sasaki: col.2, ll.47-49].

12. As to claim 2, Stevens discloses, wherein the plurality of firmware modules [module to initialize CPU, module to initialize memory] are dispatched and executed in a pre-memory execution environment prior to availability of system memory for a platform on which the BIOS is installed [col.2, 1.56 - col.3, 1.6].

13. As to claim 3, Stevens discloses calling a second module [requested BIOS module] of the plurality of firmware modules for execution during execution of a first module [dispatch manager] of the plurality of firmware modules, the second module being called by a corresponding call instruction [task] in the first module [col.5, 11.37-52].

14. As to claim 13, Stevens discloses the method comprising:

- Executing a call made by a calling agent [dispatch manager] to a first module of the plurality of firmware modules, wherein the call [task] is one of a set of calls, each call of the set of calls being associated with a module of a set of modules of the plurality of firmware modules, the associations being dependent on a configuration of the platform [col.3, 11.1-31; col.5, 11.37-52; modules required for operation].
- Starting execution of the first module of the plurality of firmware modules in response to the call [col.3, 11.1-31; col.5, 11.37-52].

- Determining which module of the set of modules is associated with the call [col.5, 11.45-52]. Starting execution of the module associated with the call [col.3, 11.1-31; col.5, 11.37-52].

15. As to claim 14, Stevens discloses the method comprising returning to the calling agent [dispatch manager] when execution of the module associated with the call is complete [col.9, 11.16-36; dispatch manager sequentially executes list of tasks with each task returning to the dispatch manager before executing next task].

16. In re claim 15, Sasaki, Stevens and ReStevens disclose each and every limitation of the claim as discussed above in reference to claim 1. Sasaki, Stevens and ReStevens disclose the method; therefore, Sasaki, Stevens and ReStevens disclose the machine readable medium comprising instructions to execute the method.

17. As to claim 16, Sasaki, Stevens and ReStevens disclose each and every limitation as discussed above in reference to claim 15. Stevens further discloses, wherein the machine comprises a platform including a processor [CPU 11] on which the instructions are executed and system memory [13], comprising instructions [from dispatched memory initializing module] that when executed by the machine cause the machine to perform an operation of initializing the system memory of the platform after the scheduled modules are dispatched [col.2, 1.48 - col.3, 1.15].

18. As to claim 17, Sasaki, Stevens and ReStevens disclose each and every limitation of the claim as discussed above in reference to claims 3 and 15.

19. As to claim 23, Sasaki, Stevens and ReStevens disclose each and every limitation of the claim as discussed above in reference to claims 13 and 15.

20. As to claim 24, Sasaki, Stevens and ReStevens disclose each and every limitation of the claim as discussed above in reference to claims 14 and 15.

21. In re claims 25-27 and 33, Sasaki, Stevens and ReStevens disclose each and every limitation of the claims as discussed above in reference to claims 15-17 and 23-24. In particular, Stevens discloses a system [computer 10a], comprising:

- A plurality of hardware components [col.5, 11.1-26, 1.54 - col.6, 1.2].
- A first memory device [12,13] to store a BIOS, the BIOS having a plurality of firmware modules [fig.2; col.4, 11.48-59; col.5, 11.27-52].
- A processor [CPU 1 1] on which the firmware modules are executed [firmware modules contain instructions that require a processor for execution], coupled to the plurality of hardware components [via PCI bus 14] and the first memory device [col.5, 11.1-26].

22. As to claims 34-35, Sasaki, Stevens and ReStevens disclose each and every limitation of the claim as discussed above in reference to claims 2, 25-27 and 33. In particular, Stevens discloses the BIOS comprising:

- A plurality of firmware modules [BIOS modules, utilities, etc.], each module of the plurality of firmware modules to provide at least one service, at least two modules providing an inter-module interface to enable each of said at least two modules to call a service provided by another module [fig.2; col.2, 1.48 - col.3, 1.15; col.8, 11.20-28; it is very well known in the art that utilities are written with interfaces enabling other modules or utilities to access a service].
- A core [inherently, some core in the broadest interpretation is needed to initiate the modules to initialize the CPU and memory] operatively coupled to the plurality of

firmware modules, wherein the core, upon operation, selects for execution a set of module from the plurality of firmware modules [fig.2; col.2, 1.48 - col.3, 1.15].

22. Claims 4-12, 18-22, 28-32, and 36-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sasaki, Stevens and ReStevens as applied to claim 3 above, and further in view of Patel, US Patent 5999989.

23. In re claim 4, Sasaki, Stevens and ReStevens disclose each and every limitation as discussed above in reference to claim 3. Sasaki, Stevens and ReStevens did not discuss the details of operation.

24. Patel discloses the method wherein calling a module [second] of the plurality of firmware modules

[col. I, 11.51-56; option ROMs associated with devices to enhance the robustness of the BIOS] comprises:

- Saving a return address of the module [col.7, 11.43-47; far return to POST].
- Determining a physical address [pointer in location] of the module [col.7, 11.1-29].
- Executing an instruction stored at the physical address of the module [col.7, 11.1-29].

Executing an instruction [performs device specific write-protection] stored at the saved return address when the module execution is complete [col.7, 11.43-47].

25. It would have been obvious to one of ordinary skill in the art, having the teachings of Sasaki, Stevens, ReStevens and Patel before him at the time the invention was made, to modify the system of Sasaki, Stevens and ReStevens to include the teachings of Patel, in order to enhance the robustness of the BIOS [Patel: col.1, 11.51-56]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to enable the BIOS to operate under different conditions.

27. As to claim 5, Patel discloses the method wherein determining the physical address of the module comprises looking up the physical address [pointer] in an import table [part of ROM header data structure] of the other module [col.7, 1.1 - col.8, 1.46].

28. As to claim 6, Patel discloses the method wherein a module of the plurality of firmware modules comprises [fig. 1 a]:

- A globally unique identifier (GUID) [72 bit serial id] to identify the firmware module [col.7, 11.4859].
- A resource list [part of ROM header data structure] to store information identifying resources needed by the firmware module to operate [col.7, 11.1-10].
- An import table [part of ROM header data structure] to store physical addresses [pointers 166, 182] of a set of modules [init, boot code] of the plurality of firmware modules that the firmware module may call during execution [col.7, 11.1-42; col.8, 11.6-46].
- A service that when executed performs a predetermined function [col.3, 1.58 - col.4, 1.10]. • An export table [interrupt table] to store a value [register argument] corresponding to a physical address of the service [col.7, 11.1 1-29; col.8, 11.6-46].
- An interface [via handle id] operatively coupled to the GUID, resource list, the service, the import table, and the export table, wherein the interface is addressable by a calling agent [POST] via the GUID to provide the calling agent access to the resource list, the service, the import table, and the export table [col.3, 1.58- col.4, 1.10].

29. As to claim 7, Patel discloses the method wherein the value [DI] stored by the export table is an offset from a start address of the firmware module [col.8, 11.26-33]. 27. As to claim 8. Patel discloses the method wherein the import table [allocation map] stores GUIDs [handle ids]

of the set of modules of the plurality of firmware modules [col.3, 1.58 col.4, 1.10; relative to POST module].

30. As to claim 9, Patel discloses the method comprising:

- Starting execution of a first module [POST] of the plurality of firmware modules [col.4, 1.46 - col.5, 1.57].
- Determining whether the first module is chainable with another module [initialization of other devices] of the plurality of firmware modules [col.7, 11.1 1-47; col.14, 11.13-26; POST makes call and returns as in a chain].
- Determining whether a hardware component [actual device] associated with the first module is present in the platform if the first module is chainable [col.6, 11.10-47].
- Completing execution of the first module if the hardware component associated with the first module is present in the platform [col.6, 11.10-47; device is activated in step 220].
- Starting execution of a second module of the plurality of firmware modules without completing execution of the first module if the hardware component associated with the first module is not present in the platform [fig.2; col.6, 11.10-47; if device is not present, steps 206-208 are repeated with first device taken out of allocation map and second device being executed instead].

31. As to claim 10, Patel discloses the method wherein the first module includes a data structure [allocation map] to store a physical address of the second module [col.3, 1.58 - col.4, 1.10].

32. As to claim 11, Patel discloses each and every limitation of the claim as discussed above in reference to claim 9. Furthermore, Patel discloses multiple firmware modules that can be chained by one with ordinary skill in the art [fig.5c].

33. As to claim 12, Stevens discloses the method wherein completing execution of the second module [task associated with module] further comprises returning to a calling agent [dispatch manager] that called the first module [col.9, 11.16-36; dispatch manager sequentially executes list of tasks with each task returning to the dispatch manager before executing next task].

34. In re claims 18-22, Patel, Sasaki, Stevens and ReStevens disclose each and every limitation of the claims as discussed above in reference to claims 4-12 and 15.

35. In re claims 28-32, Patel, Sasaki, Stevens and ReStevens disclose each and every limitation of the claims as discussed above in reference to claims 4-12 and 25.

36. In re claims 36-41, Patel, Sasaki, Stevens and ReStevens disclose each and every limitation of the claims as discussed above in reference to claims 4-12 and 34.

Response to Arguments

37. Examiner acknowledges Applicant's stipulation dated June 8, 2006 concerning the provisional double patenting rejection [pg.12 of Remarks]. Examiner will maintain the rejection until the co-pending application 10/112920 issues and the issued claims do not warrant a nonstatutory double-patenting rejection in the instant application.

38. Applicant's arguments filed June 8, 2006 have been fully considered but they are not persuasive. Applicant alleges that the "firmware modules in Stevens are code rather than the non-solid state system such as ROM... firmware modules in ReStevens as the non-solid state system such as ROM, the combination of Stevens and ReStevens is no operable". Examiner disagrees and submits that Applicant correctly concedes that both Stevens and ReStevens teach firmware modules operable in either solid or non-solid state systems.

39. Applicant's other arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

40. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hsiung, "EFI Training Session" discloses some implementation details of EFI.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tse Chen
July 6, 2006



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